REMARKS

This Amendment responds to the Office Action dated February 21, 2007 in which the Examiner rejected claims 1, 4-6, 10 and 13-17 under 35 U.S.C. §103.

As indicated above, claims 1, 6, 10 and 15 have been amended in order to make explicit what is implicit in the claims. The amendment is unrelated to a statutory requirement for patentability and does not narrow the literal scope of the claims.

Claims 1, 6 and 10 claim an image processing apparatus and method in which an error diffusion processing is performed using a threshold value. In claims 1 and 10, error diffusion processing clears the error memory of the pixel of interest so that calculation of error and distribution of the error for the white pixel is not performed. In claim 6, the error diffusion processing clears the error memory of the pixel of interest so that calculation of an error and distribution of the error to black pixels is not performed.

Through the method and apparatus having an error diffusion process which clears the error memory of the pixel of interest so that calculation of error and subsequent distribution of the error to pixels is not performed, as claimed in claims 1, 6 and 10, the claimed invention provides an image processing apparatus which enables high speed image processing without degrading image quality. The prior art does not show, teach or suggest the invention as claimed in claims 1, 6 and 10.

Claim 15 claims an image processing apparatus including an error diffusion processing unit which outputs a signal representing a white or black pixel and clears the error memory of the pixel of interest so that calculation of error and subsequent distribution of errors to the white or black pixel is not performed. The error diffusion

processing unit performs error diffusion process using a single threshold value in a binarization process and changes the threshold value based on a relationship between the input and the threshold value. The relationship is that the threshold value increases depending on the increase of the input.

Through the structure of the claimed invention having an error diffusion processing which clears an error memory of the pixel of interest for a white or black pixel so that calculation of an error and subsequent distribution of the error to pixels is not performed, as claimed in claim 15, the claimed invention provides an image processing apparatus which enables high speed image processing without the degrading image quality. The prior art does not show, teach or suggest the invention as claimed in claim 15.

Claims 1, 4-6, 10 and 13-17 were rejected under 35 U.S.C. §103 as being unpatentable over *Ishiguro et al.* (U.S. Patent 6,501,566) in view of *Engineering Design Choice*.

Ishiguro et al. appears to disclose an image processing apparatus employing a multi-value error diffusion process. (Column 1, lines 9-10). An error diffusion process is carried out, if necessary, by error diffusion processing unit 106-07. In the error diffusion process, pixel density D of the image data output from MTF correction unit 106-06 and a reference density S output from control unit 106-12 are used. Converted pixel density P of the image data subjected to an error diffusion process is output from error diffusion processing unit 106-07. (Column 6, lines 23-30). FIG. 3 is a block diagram showing a structure of error diffusion processing unit 106-07 of FIG. 2. Referring to FIG. 3, an error diffusion processing unit 106-07 includes an adder 41, a tone convertor 42, a subtractor 43, an error addition matrix 44, an error

memory 45, and an address counter 46. (Column 6, lines 38-43). The image processing apparatus of the present embodiment is characterized in that the values of reference densities S1 and S2 are altered according to the density histogram of the input image data. (Column 7, lines 13-16).

Thus, *Ishiguro et al.* merely discloses in Fig. 3 performing an error diffusion processing even if an input signal D is zero. In other words, the input signal D is input to the adder 41 regardless of the value of the input signal D. The adder 41 adds a correction value R to the input signal D to generate a signal D' as corrected. The correction value R is an error generated from values of surrounding pixels. Therefore, if a pixel of a value other than zero is generated, the error would be diffused and thus zero is not readily reached. It is thus apparent that *Ishiguro et al.* performs the addition of the correction value R and subsequent error diffusion even if the input signal D is zero. Thus, nothing in *Ishiguro et al.* shows, teaches or suggests clearing an error memory of a pixel of interest so that calculation of an error and subsequent distribution of the error to pixels is not performed, as claimed in claims 1, 6, 10 and 15. Rather, *Ishiguro et al.* teaches away from the claimed invention and performs an error diffusion process even if the input signal is zero.

Applicant respectfully traverses the Examiner's statement that it would be an obvious engineering design choice to simply not perform the error and error distribution calculations when the input pixel is zero. Nothing in any of the references shows, teaches or suggests clearing an error memory of a pixel of interest so that calculation of error and subsequent distribution of the error to pixels is not performed. Furthermore, a generated error does not easily and immediately become zero even if the input pixel value is zero because errors are diffused from

other pixels. Furthermore, *Ishiguro et al.* clearly discloses generating a corrected signal by adding a correction value. Nothing in *Ishiguro et al.* shows, teaches or suggests clearing the error memory. In fact, *Ishiguro et al.* clearly teaches performing error diffusion processing even if the input signal is zero.

Since nothing in *Ishiguro et al.* or *Design Choice* shows, teaches or suggests clearing an error memory of a pixel of interest so that calculation of an error and subsequent distribution of the error to pixels is not performed as claimed in claims 1, 6, 10 and 15, Applicant respectfully requests the Examiner withdraws the rejection to claims 1, 6, 10 and 15 under 35 U.S.C. §103.

Claims 4-5, 13-14 and 16-17 depend from claims 1, 10 and 15 and recite additional features. Applicant respectfully submits that the claims 4-5, 13-14 and 16-17 would not have been obvious within the meaning of the 35 U.S.C. §103 over *Ishiguro et al.* and *Design Choice* at least for the reasons as set forth above. Therefore, Applicant respectfully requests the Examiner withdraws the rejection to claims 4-5, 13-14 and 16-17 under 35 U.S.C. §103.

Thus it now appears that the application is in condition for reconsideration and allowance. Reconsideration and allowance at an early date are respectfully requested.

If for any reason the Examiner feels that the application is not now in condition for allowance, the Examiner is requested to contact, by telephone, the Applicant's undersigned attorney a t the indicated telephone number to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed within the currently set shortened statutory period, Applicant respectfully petitions for an appropriate extension of time.

The fees for such extension of time may be charged to Deposit Account No. 02-4800.

In the event that any additional fees are due with this paper, please charge our Deposit Account No. 02-4800.

Respectfully submitted,

BUCHANAN INGERSOLL & ROONEY PC

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